CLAIMS

We claim:

1. A method for accessing hardware resources in a computer system, comprising:
   (a) assigning a first I/O resource a first physical resource address;
   (b) assigning a second I/O resource a second physical resource address;
   (c) dynamically routing a virtual resource address between said first and second physical resource addresses.

2. The method of claim 1, wherein the step of dynamically routing said virtual resource address includes providing a hardware resource map for logically storing said virtual resource address and at least one of said first and second physical resources addresses.

3. The method of claim 1, wherein the step of dynamically routing said virtual resource address includes redirecting said virtual resource address from said first physical resource address to said second physical resource address.

4. The method of claim 3, further comprising renumbering nodes in an existing hardware resource map.

5. The method of claim 4, wherein said renumbering step is implemented globally.

6. The method of claim 1, wherein the step of dynamically routing said virtual resource address includes changing a hardware resource map at run time.

7. The method of claim 1, wherein the physical resource addresses are on different nodes of the computer system.

8. The method of claim 1, wherein the system is a multiprocessor system including at least two nodes each having at least one processor.

9. The method of claim 1, wherein the step of dynamically routing said virtual resource address includes mapping said virtual resource address to said physical resource address using firmware of said system.

10. The method of claim 1, wherein the step of dynamically routing said virtual resource address includes using a system interconnect.

11. The method of claim 10, wherein the system interconnect is a NUMA interconnect.

12. The method of claim 11, wherein the step of dynamically routing said virtual resource address includes mapping said virtual resource address to said physical resource address using firmware of said interconnect.

13. The method of claim 1, wherein the first I/O resource and a non-I/O resource are collectively assigned said first physical resource address.

14. A computer system comprising:
platform firmware having a virtual resource address and a physical resource address;
a first I/O resource having a first physical resource address;
a second I/O resource having a second physical resource address; and
a manager to translate said virtual address to one of said first and second physical resource addresses.

15. The system of claim 14, further comprising a hardware resource map to logically store said virtual address and at least one of said first and second physical resource addresses.

16. The system of claim 14, wherein said manager redirects said virtual resource address from said first physical resource address to said second physical resource address.

17. The system of claim 16, wherein said manager renumbers nodes in an existing hardware resource map.

18. The system of claim 17, wherein said manager comprises an instruction to globally renumber said nodes.

19. The system of claim 15, further comprising an instruction to change said hardware resource map at run time.

20. The system of claim 14, wherein said physical resource addresses are on different nodes of said computer system.

21. The system of claim 14, wherein the system is a multiprocessor system including at least two nodes each having at least one processor.

22. The system of claim 14, wherein said manager maps said virtual resource address to said physical resource address using firmware of said system.

23. The system of claim 14, wherein said manager routes said virtual address through an interconnect.

24. The system of claim 23, wherein said interconnect is a NUMA interconnect.

25. The system of claim 24, wherein said manager maps said virtual resource address to said physical resource address using firmware of said interconnect.

26. The system of claim 14, wherein said first I/O resource and a non-I/O resource are a collectively assigned said first physical resource address.

27. An article comprising:

a computer-readable signal bearing medium readable by a computer having multiple nodes;

platform firmware having an address for a virtual resource and an address for a physical resource;

means in the medium for dynamically routing fixed address references; and

means in the medium for logically storing said physical and virtual resource addresses.

28. The article of claim 27, wherein the medium is selected from the group consisting of a recordable data storage medium, and a modulated carrier signal.

29. The article of claim 27, wherein said logical storing means is a hardware resource map.

30. The article of claim 27, further comprising a manager to translate said resource address and to redirect said virtual address to a physical hardware address.

31. The article of claim 30, wherein said dynamic routing means comprises an instruction for renumbering nodes in said logical storing means.

32. The article of claim 27, wherein said dynamic routing means comprises an instruction to change said logical storing means at run time.

33. A method for accessing hardware resources in a computer system, comprising:

(a) assigning a first I/O resource a first physical resource address;

(b) assigning a second I/O resource a second physical resource address;

(c) providing a hardware resource map for storing a virtual resource address and said first and second physical resource addresses; and

(d) dynamically routing said virtual resource address between said first and second physical resource addresses.